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Attorney Docket No. 0756-2294

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MEMO 0756-2294; SN 09/832,867

100264010055002707100000258129510

-) Group Art Unit: 2822
-) Examiner: M. Lewis

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visions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, PTO-1449 listing references known to Applicant and made of record in the above identified application. e submitted herewith in accordance with 37 C.F.R.

directed to U.S. Patent Application Nos. 09/454,146 to the present patent application.

180 is being submitted to comply with the provisions

/ authorized to charge fees under 37 C.F.R. §§1.16, and 1.20(d) (except the Issue Fee) which may be any overpayment to Deposit Account No. 50-2280.

2822
28



Attorney Docket No. 0756-2294

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shunpei YAMAZAKI et al.

Serial No. 09/832,867

Filed: April 12, 2001

For: LIGHT EMITTING DEVICE

COMPRISING THIN FILM

TRANSISTOR WITH DISTINCT

POSITION OF GATE ELECTRODE

AND IMPURITY REGIONS

) Group Art Unit: 2822

) Examiner: M. Lewis

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Honorable Commissioner of Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The Examiner's attention is directed to U.S. Patent Application Nos. 09/454,146 and 10/386,257 which are related to the present patent application.

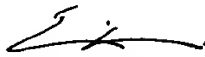
A check in the amount of \$180 is being submitted to comply with the provisions of 37 C.F.R. § 1.97(c).

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Respectfully submitted,



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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Complete if Known

Application Number	09/832,867
Filing Date	April 12, 2001
First Named Inventor	Shunpei YAMAZAKI, et al.
Group Art Unit	2822
Examiner Name	Monica Lewis
Attorney Docket Number	0756-2294

Sheet

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U.S. PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		4,963,504		Huang	10/16/90	
		5,323,042		Matsumoto	06/21/94	
		5,399,502		Friend et al.	03/21/95	
		5,412,240		Inoue et al.	05/02/95	
		5,532,175		Racanelli et al.	07/02/96	
		5,543,340		Lee	08/06/96	
		5,543,947		Mase et al.	08/06/96	
		5,583,067		Sanchez	12/10/96	
		5,581,092		Takemura	12/03/96	
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		5,594,569		Konuma et al.	01/14/97	
		5,637,519		Tsai et al.	06/10/97	
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		5,858,867		Hsai et al.	01/12/99	
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		5,923,961		Shibuya et al.	07/13/99	
		6,153,445		Yamazaki et al.	11/28/00	
		6,166,397		Yamazaki et al.	12/26/00	
		6,166,414		Miyazaki et al.	12/26/00	
		6,198,133		Yamazaki et al.	03/06/01	
		6,211,536		Zhang	04/03/01	
		6,259,138		Ohtani et al.	07/10/01	
		6,274,400		Jen	08/14/01	
		6,274,887		Yamazaki et al.	08/14/01	
		6,277,679		Ohtani	08/21/01	

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Group Art Unit	2822
Examiner Name	Monica Lewis
Attorney Docket Number	0756-2294

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		Number	Kind Code ² (if known)			
		6,281,552		Kawasaki et al.	08/28/01	
		6,284,577		Suzawa et al.	09/04/01	
		6,303,963		Ohtani et al.	10/16/01	
		6,306,694		Yamazaki et al.	10/23/01	
		6,337,731		Takemura	01/08/02	
		6,346,730		Kitakado et al.	02/12/02	
		6,358,766		Kasahara	03/19/02	
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		6,384,808		Azami	05/07/02	
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		6,399,988		Yamazaki	06/04/02	
		6,407,430		Ohtani et al.	06/18/02	
		6,420,200		Yamazaki et al.	07/16/02	
		6,469,317		Yamazaki et al.	10/22/02	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		US Patent Application Serial No. 10/386,257 including specification, drawings, claims, and filing receipt; filed March 11, 2003; Inventor: Hideto Ohnuma.	
		US Patent Application Serial No. 09/454,146 including specification, drawings, claims, and filing receipt; filed December 3, 1999; Inventors: Shunpei YAMAZAKI, et al.	
		Yoshida et al., "A Full-Color Thresholdless Antiferroelectric LCD Exhibiting Wide Viewing Angle with Fast Response Time," SID 97 DIGEST, pp. 841-844.	ENG
		Hwang et al., "High Performance Submicron SOI/CMOS with an Elevated Source/Drain Structure," PROCEEDINGS OF THE ANNUAL SOS/SOI TECHNOLOGY CONFERENCE, IEEE, Vol. 19, 1993, pp. 132-133.	ENG
		Choi et al., "Gate-Overlapped Lightly Doped Drain Poly-Si Thin-Film Transistors for Large Area-AMLCD," IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 45, No. 6, June, 1998, pp. 1272-1279.	ENG

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Filing Date	April 12, 2001
First Named Inventor	Shunpei YAMAZAKI, et al.
Group Art Unit	2822
Examiner Name	Monica Lewis
Attorney Docket Number	0756-2294

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FOREIGN PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
		JP	04-369271		Takeda et al.	12/22/92		FULL
		JP	05-102483		Ueda	04/23/93		FULL
		JP	06-037314		Tsuchimoto	02/10/94		AB
		JP	07-202210		Taniguchi	08/04/95		AB
		JP	08-078329		Otani	03/22/96		AB
		JP	08-051207		Sato	02/20/96		AB
		JP	08-110530		Koyama et al.	04/30/96		AB
		JP	10-135469		Yamazaki et al.	05/22/98		AB
		JP	10-144929		Shibuya et al.	05/29/98		AB
		EP	0 451 968		Coxon	10/16/91		ENG
		JP	10-247735		Takano et al.	09/14/98		AB
		EP	0 803 911		Adan et al.	10/29/97		ENG
		JP	10-135468		Yamazaki et al.	05/22/98		AB

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		Tanaka, et al., "Ultrafast Operation of V _{th} -Adjusted p ⁺ -n ⁺ Double-Gate SOI MOSFET'S," IEEE Electron Device Letters, Vol. 15 (Oct., 1994), No. 10, pp. 386-388.	ENG
		Inui et al., "Thresholdless Antiferroelectricity in Liquid Crystals and its Application to Displays," J. Mater Chem., 1996, 6(4), pp. 671-673.	ENG
		Takada, et al., PROCEEDINGS OF 46 TH SPRING MEETINGS OF THE SOCIETY FOR APPLIED PHYSICS OF JAPAN, 28P-V-8, page 1316.	NONE
		Hwang et al., "Novel Polysilicon/TiN Stacked-Gate Structure for Fully-Depleted SOI/CMOS," IEDM '92, pp. 345-348.	ENG
		Yoshihara, EKISHO, Vol. 3, No. 3, pp. 190-194.	NONE
		Furue et al., "P-78: Characteristics and Driving Scheme of Polymer-Stabilized Monostable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability," SID '98 DIGEST, pp. 782-785.	ENG
		Hatano et al, "A Novel Self-Aligned Gate-Overlapped LDD Poly-Si TFT with High Reliability and Performance," IEDM '97, pp. 523-526.	ENG

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